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Claims

[c1] What is claimed is:

1. A method for fabricating a thin film transistor (TFT) of a liquid crystal display (LCD), the method comprising the steps of:

providing a substrate;

sequentially depositing a transparent conductive layer, a first metal layer, a first insulating layer, a semiconductor layer, and a second metal layer on the substrate;

performing a first photo-etching-process (PEP) to remove portions of the second metal layer, the semiconductor layer, the first insulating layer, the first metal layer, and the transparent conductive layer to form a source electrode, a drain electrode and a channel region;

depositing a second insulating layer and performing a second PEP to remove portions of the second insulating layer to form a plurality of contact holes; and

depositing a third metal layer for electrically connecting the source electrode and the drain electrode with other wires, depositing a passivation layer for protecting the third metal layer, and performing a third PEP to remove portions of the third metal layer and the passivation layer.

[c2] 2. The method of claim 1 wherein the substrate comprises a glass substrate, a quartz substrate, or a plastic substrate.

[c3] 3. The method of claim 1 wherein the first metal layer, the second metal layer and the third metal layer comprise tungsten (W), chromium (Cr), aluminum (Al), copper (Cu), molybdenum (Mo),or an alloy of any of the above metals.

[c4] 4. The method of claim 1 wherein the transparent conductive layer comprises an indium tin oxide (ITO) or an indium zinc oxide (IZO).

[c5] 5. The method of claim 1 wherein the first PEP includes a first halftone photolithograph process, the first halftone photolithograph process forming a first photoresistor layer and a second photoresistor layer on the second metal layer.

[c6] 6. The method of claim 1 wherein the second PEP includes a second halftone photolithograph process.

[c7] 7. The method of claim 1 wherein step of performing the second PEP further comprises:
performing a second halftone photolithograph process to form a third photoresistor layer and a fourth photore-

sistor layer on the second insulating layer;
removing portions of the second insulating layer, the semiconductor layer, the first insulating layer and the first metal layer uncovered by the third photoresistor layer and the fourth photoresistor layer;
removing the fourth photoresistor layer; and
removing portions of the second insulating layer to form the contact holes.

[c8] 8. The method of claim 1 wherein step of performing the second PEP further comprises:
forming a third photoresistor layer on the second insulating layer;
removing portions of the second insulating layer, the semiconductor layer, the first insulating layer, and the first metal layer uncovered by the third photoresistor layer or by the second metal layer.

[c9] 9. The method of claim 8 wherein the second PEP includes a wet-etching process with a predetermined selectivity.

[c10] 10. A method for fabricating a liquid crystal display (LCD), the method comprising the steps of:
providing a substrate;
sequentially depositing a transparent conductive layer, a first metal layer, a first insulating layer, a semiconductor

layer, and a second metal layer on the substrate;
performing a first photo-etching-process (PEP) to remove portions of the second metal layer, the semiconductor layer, the first insulating layer, the first metal layer, and the transparent conductive layer to form a gate line and a common line, and define a TFT region, a channel region and a pixel electrode region;
depositing a second insulating layer and performing a second PEP to remove portions of the second insulating layer, the semiconductor layer, the first insulating layer, and the first metal layer to form a plurality of contact holes and expose portions of the transparent conductive layer; and
depositing a third metal layer and a passivation layer, and performing a third PEP to form a data line and a capacitance region, and electrically connect the TFT region and the pixel electrode region.

[c11] 11. The method of claim 10 wherein the substrate comprises a glass substrate, a quartz substrate, or a plastic substrate.

[c12] 12. The method of claim 10 wherein the first metal layer, the second metal layer and the third metal layer are composed of tungsten (W), chromium (Cr), aluminum (Al), copper (Cu), molybdenum (Mo),or an alloy of any of the above metals.

[c13] 13. The method of claim 10 wherein the transparent conductive layer comprises an indium tin oxide (ITO) or an indium zinc oxide (IZO).

[c14] 14. The method of claim 10 wherein the first PEP includes a first halftone photolithograph process, the first halftone photolithograph process forming a first photoresistor layer and a second photoresistor layer on the second metal layer.

[c15] 15. The method of claim 10 wherein the second PEP includes a second halftone photolithograph process.

[c16] 16. The method of claim 10 wherein step of performing the second PEP further comprises:
performing a second halftone photolithograph process to form a third photoresistor layer and a fourth photoresistor layer on the second insulating layer;
removing portions of the second insulating layer, the semiconductor layer, the first insulating layer and the first metal layer uncovered by the third photoresistor layer and the fourth photoresistor layer;
removing the fourth photoresistor layer; and
removing portions of the second insulating layer to form the contact holes.

[c17] 17. The method of claim 10 wherein step of performing

the second PEP further comprises:

forming a third photoresistor layer on the second insulating layer;

removing portions of the second insulating layer, the semiconductor layer, the first insulating layer, and the first metal layer uncovered by the third photoresistor layer or by the second metal layer.

[c18] 18. The method of claim 17 wherein the second PEP includes a wet-etching process with a predetermined selectivity.

[c19] 19. The method of claim 10 wherein the third metal layer strides across the common line to electrically connect two pixel electrode regions.